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FPGA Implementation of Selective Harmonic Elimination Controlled Asymmetrical Cascaded Nine Levels Inverter Using Newton Raphson Algorithm

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***Abstract*— Asymmetrical structure is used to reduce the number of bridges and gate drive circuits and DC sources. This structure therefore provides the capability to produce higher voltages at higher speeds with low switching frequency which has inherent low switching losses and high converter efficiency.**
Newton Raphson (N-R) algorithm is investigated for the selective harmonic elimination (SHE) to calculate switching angles for a range of variation for the modulation rate 'r' for an asymmetrical cascaded multilevel inverter control.
Based on simulation studies, performance of the proposed algorithm for a nine levels asymmetrical cascaded H-bridge inverter, is evaluated and experimentally tested on an prototype using FPGA to implement SHE based on NR algorithm.

***Keywords*— Asymmetrical CHB multilevel inverter, Newton Raphson algorithm, Switching angles, SHE, THD, FPGA.**

I. INTRODUCTION

Among the various types of multilevel inverter topologies, the cascaded H-bridge (CHB) has attracted special attention due to its modular structure, which provides high reliability and better fault tolerance. Increasing the number of levels is also easier with minimal modifications in the hardware and control algorithm. Therefore, the CHB multilevel inverter has become popular in renewable energy (solar/wind power inverters), and motor-drive applications up to MegaWatt (MW) power levels. For these applications, the converter output voltage must respect the requirement for maximum voltage and current THD as specified in IEEE Std.519-1992[1], [2].

In this paper, asymmetric multilevel inverter is used, with different DC source in each cell (HB). Compared to a symmetric H-bridge topology, it is possible to increase the number of output voltage levels and produce a better sinusoidal waveform.

Several methods are put forth for the harmonic elimination in literature. The methods proceeds from the basic sinusoidal pulse width modulation (SPWM) which are not able to eliminate lower harmonics completely [3] and space vector modulation (SVM) where the application of SVM in cascaded topologies is usually limited to a small number of levels due to the large number of switching vectors [4], [5].

Selective harmonic elimination pulse width modulation (SHE PWM) is employed in multilevel inverters which require solving the non linear equations in order to eliminate certain harmonic orders by the generation of switching angles corresponding to harmonic elimination.

In fact many studies have been carried out to find optimal angles using optimization techniques such as polynomial resultants theory (PRT) [6] or genetic-algorithm (GA) [7]. In the PRT solution, when the voltage levels of multilevel inverters are high, the resulting high order polynomial terms can no longer be solved. In a GA-based method, the main challenge is that the result may fall into the trap of local minimums. Therefore, despite its considerable efficiency for large dimension optimization problems, it cannot guarantee the best optimized result [3].

In this paper selective harmonic elimination technique is implemented using Newton Raphson algorithm. This method has better computational efficiency and exhibits more stable convergence characteristic. It is considerably more robust than other optimization methods without any extra computational burden.

Many researches chose to implement switching angles by digital signal processor (DSP) or microcontroller (MCU). This approach has the advantages of simple circuitry, software realization and flexibility. However, there are also several disadvantages [5], [6]. As the levels of the inverter increase and the inverter structure becomes more complex, the programming of the corresponding switching angles in the DSP or MCU becomes one of the most time-consuming tasks [5]. If the DSP or MCU is not able to provide enough on-chip peripherals, such as comparators and dead-time controllers to support the control signals outputs, extra hardware circuits need to be designed to cooperate with the controller.

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An attractive idea is to implement the switching angles via an application-specific integrated circuit (ASIC). The field programmable gate array (FPGA) is a sub-class of ASIC controllers which provides characteristics such as fast prototyping, simple hardware and software design and higher switching frequency [8]. FPGAs development reached a level of maturity that made them the choice of implementation in many fields [3]. To solve the problems mentioned above and to provide easy, fast and steady control, switching angles are analyzed and implemented into FPGA memories to control asymmetrical cascaded nine levels inverter.

This paper is organized as follows. Section 2 describes power topology of cascade multilevel inverter. Harmonic elimination problem in CHB multilevel inverter based on NR optimization is explained in section 3. Simulation and experimental results are presented in section 4 and 5 respectively. Finally, the concluding remarks are drawn in section 6.

II. POWER TOPOLOGY OF ASYMMETRIC CASCADED H-BRIDGE MULTILEVEL INVERTER

The cascaded multilevel inverter is one of several multilevel configurations. It is formed by connecting single-phase H-bridges inverters in series as shown in figure 1. In symmetrical cascaded multilevel inverter, where the DC-link voltages of HBs are identical. The number of output levels is normalized by:

$$N = 2h + 1, \quad \text{h: number of H-Bridge} \tag{1}$$

When the number of HB (h=2), as shown in figure1, therefore the single phase symmetric inverter output voltage V_{AO} gives a five levels output voltage : $N = 2 * 2 + 1 = 5$.

For asymmetrical cascade multilevel inverter where the DC-link voltages of the 2 HBs are unequal the numbers of output level are normalized by:

$$N = 2(\sum_{j=1}^{h} \lambda j) + 1 , \quad \lambda j = \frac{Vdcj}{Vdc1} \tag{2}$$

Asymmetrical nine levels HB inverter, is obtained for Vdc2= 3Vdc1=3E : $N = 2(1 + 3) + 1 = 9$.

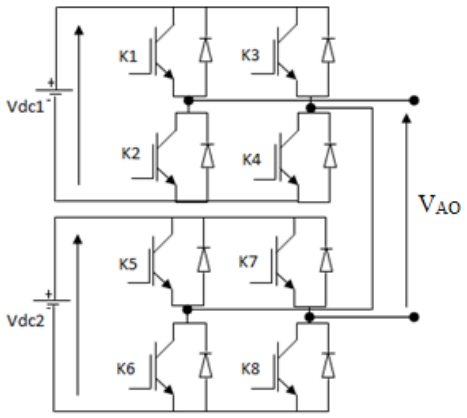

Fig.1 Topology of single phase Asymmetrical Cascaded multilevel inverter

We can notice that, for the same number of bridges, the asymmetrical structure compared to a symmetrical H-bridge topology, can produces a higher number of levels, consequently a better voltage quality, which make the asymmetrical inverter to be a perfect candidate for selective harmonic elimination « SHE ».

III. HARMONIC ELIMINATION BASED ON NEWTON RAPHSON ALGORITHM

In this section staircase voltage waveform as shown in figure 2 is chosen for the selective harmonic elimination (SHE) technique in nine levels H-bridge inverters [9].

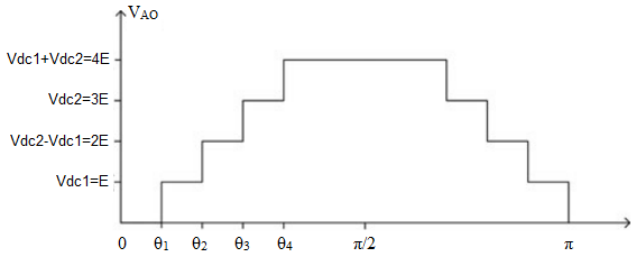

Fig.2 Staircase CHB multilevel inverter output voltage

Because of the quarter-wave symmetry, the Fourier series expansion of the output voltage V_{AO}, as shown in Figure 2, can be written as:

$$V_{AO}(\omega t) = \sum_{n=1}^{+\infty} A_n sin(n\omega t) \tag{3}$$

p and A_n are the number of switching angles and the magnitude of the n^{th} harmonic order respectively, such as:

$$A_n = \frac{4E}{n\pi} \sum_{i=1}^{p} cos(n\theta_i) \tag{4}$$

For N levels, in the staircase output voltage waveform, the number of the switching angles p to be calculated is given by:

$$p = \frac{N-1}{2} \tag{5}$$

For a nine level inverter output voltage (N=9), the number of harmonics to be eliminated is equal to (p-1) =3.

The maximum fundamental voltage is obtained when all the switching angles are zero.

In this case:

$$A_{1max} = \frac{4p}{\pi} V_{dc1} = \frac{16}{\pi} E \tag{6}$$

It is desirable to control the fundamental component of the output voltage at a certain value and eliminate the low-order harmonics as much as possible. In a three-phase and three-wire system the triplen harmonics will be automatically eliminated. In fact, p switching angles are determined by imposing the amplitude of the fundamental component and eliminate the (p-1) harmonics.

In our case, the four switching angles (θ1, θ2, θ3 and θ4) must be determined to eliminate the first three odd harmonic components (5^{th}, 7^{th} and 11^{th} order) [10]. One solution

approach for sets of nonlinear transcendental equations (4) is by applying an iterative method based one Newton Raphson algorithm [11].

$$\begin{cases} cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) = r * \pi \\ cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) = 0 \\ cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) = 0 \\ cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) = 0 \end{cases} \quad (7)$$

Modulation rate **r** is given as follow:

$$r = \frac{A_1}{pV_{dc1}} = \frac{A_1}{pE} \quad \text{: Modulation rate} \quad (8)$$

The Newton_Raphson (NR) method is one of the fastest iterative methods. Here, the NR is used in Matlab to solve the set of transcendental equations in (7), and the following matrices are implemented [12]:

The switching angle matrix,

$$\theta^j = \begin{bmatrix} \theta_1^j \\ \theta_2^j \\ \theta_3^j \\ \theta_4^j \end{bmatrix} \quad (9)$$

The nonlinear system matrix,

$$F(\theta) = \begin{bmatrix} cos(\theta_1) & cos(\theta_2) & cos(\theta_3) & cos(\theta_4) \\ cos(5\theta_1) & cos(5\theta_2) & cos(5\theta_3) & cos(5\theta_4) \\ cos(7\theta_1) & cos(7\theta_2) & cos(7\theta_3) & cos(7\theta_4) \\ cos(11\theta_1) & cos(11\theta_2) & cos(11\theta_3) & cos(11\theta_4) \end{bmatrix} \quad (10)$$

And,

$$\left[\frac{\partial F}{\partial \theta}\right]^j = -\begin{bmatrix} sin(\theta_1^j) & sin(\theta_2^j) & sin(\theta_3^j) & sin(\theta_4^j) \\ 5sin(5\theta_1^j) & 5sin(5\theta_2^j) & 5sin(5\theta_3^j) & 5sin(5\theta_4^j) \\ 7sin(7\theta_1^j) & 7sin(7\theta_2^j) & 7sin(7\theta_3^j) & 7sin(7\theta_4^j) \\ 11sin(11\theta_1^j) & 11sin(11\theta_1^j) & 11sin(11\theta_3^j) & 11sin(11\theta_3^j) \end{bmatrix} \quad (11)$$

The corresponding harmonic amplitude matrix,

$$T = \begin{bmatrix} r\pi \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (12)$$

Generally, equation (7) can be written:

$$F(\theta) = T \quad (13)$$

By using matrices (8) to (13) and the Newton_Raphson method, the statement of algorithm is shown as follows:

- Guess a set of initial values for θ^j with j = 0

Assume, $$\theta^0 = \begin{bmatrix} \theta_1^0 \\ \theta_2^0 \\ \theta_3^0 \\ \theta_4^0 \end{bmatrix} \quad (14)$$

- Calculate the value of

$$F(\theta^0) = F^0 \quad (15)$$

- Linearize equation (10) about θ^0

$$F^0 + \left[\frac{\partial F}{\partial \theta}\right]^0 d\theta^0 = T \quad (16)$$

And,

$$d\theta^0 = \begin{bmatrix} d\theta_1^0 \\ d\theta_2^0 \\ d\theta_3^0 \\ d\theta_4^0 \end{bmatrix} \quad (17)$$

- Solve $d\theta^0$ from equation (16),

$$d\theta^0 = INV\left[\frac{\partial F}{\partial \theta}\right]^0 (T - F^0) \quad (18)$$

Where $INV\left[\frac{\partial F}{\partial \theta}\right]^0$ is the inverse matrix of $\left[\frac{\partial F}{\partial \theta}\right]^0$

- As updated the initial values,

$$\theta^{j+1} = \theta^j + d\theta^j \quad (19)$$

Repeat the process for equations (15) to (19), until $d\theta^j$ is satisfied to the desired degree of accuracy, and the solutions must satisfy the condition:

$$\theta_1 < \theta_2 < \theta_3 < \theta_4 < \frac{\pi}{2} \quad (20)$$

IV. SIMULATION RESULTS

By using MATLAB program, NR technique returns all the possible combinations of the switching angles for different values of **r**. The result is represented by fig.3, where one can see the presence of unique solutions of angles for $0.826 \leq r \leq 0.9$ and for $0.925 \leq r \leq 1.0$. On the other side, the system does not accept any solution.

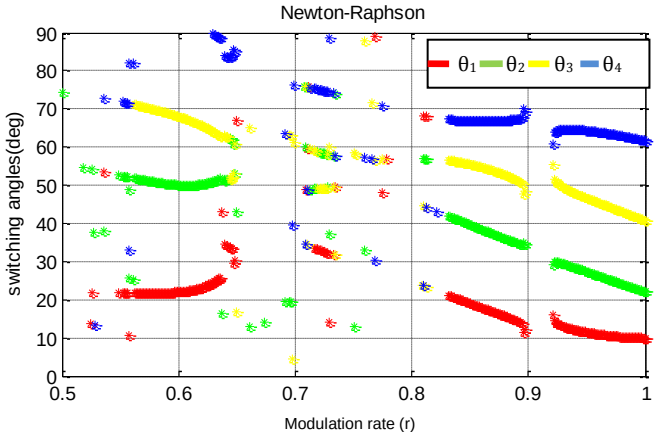

Fig.3 Switching angles versus modulation rate based on NR algorithm

Single phase asymmetrical cascaded nine levels inverter is used to drive R-L load (R =220Ω, L= 0.5mH) such as the first HB inverter unit (HB1) and the second HB inverter unit (HB2) DC sources voltages are Vdc1=E= 50V and Vdc2= 3E= 150V respectively and the modulation rate is chosen to be equal to 1(r=1) and output voltage frequency: f=50 Hz.

As result, figure 3 gives the four switching angles obtained by NR algorithm such, θ1 = 10.01, θ2 = 22.14, θ3 = 40.75, θ4 = 61.75. Figure 4.a and 4.b represent the commutation cells HB1 and HB2 simulation control signals results for the four switching angles and modulation rate given above.

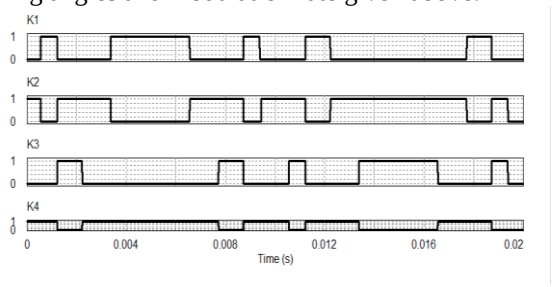

Fig.4.a HB1 commutation cells control signals based on NR algorithm

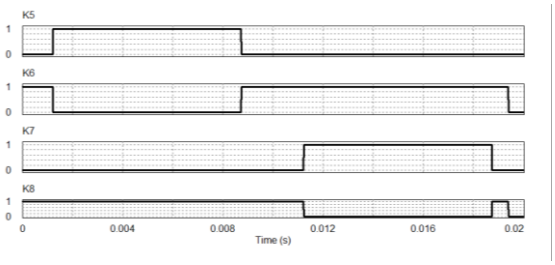

Fig.4.b HB2 commutation cells signal control based on NR algorithm

Using Matlab-Simulink, asymmetrical nine levels HB inverter simulation output voltage and its FFT analysis based on NR and equal calculated switching angles (ECSA) technique are depicted in Figures 5.a, 5.b, and figure 6.a,6.b respectively.

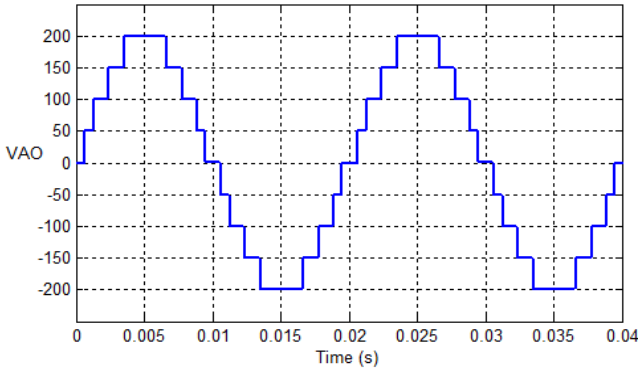

Fig.5.a Single phase nine level inverter output voltage wave form (V_{AO}) based on NR Algorithm

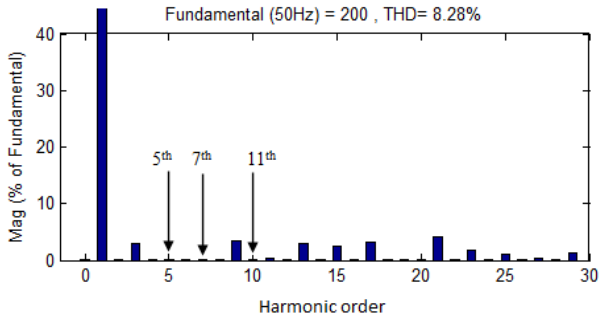

Fig.5.b FFT analysis of the nine level output voltage waveform (V_{AO}) based on NR algorithm

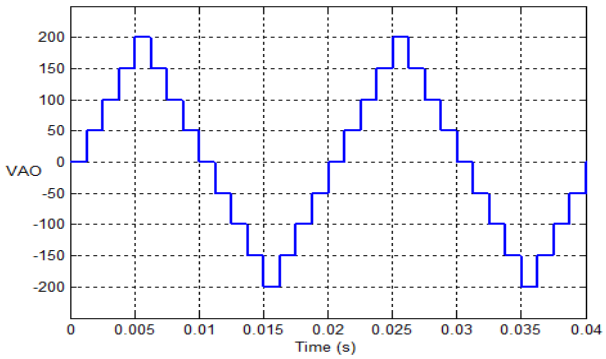

Fig.6.a. Single phase nine level inverter output voltage waveform (V_{AO}) based on ECSA technique

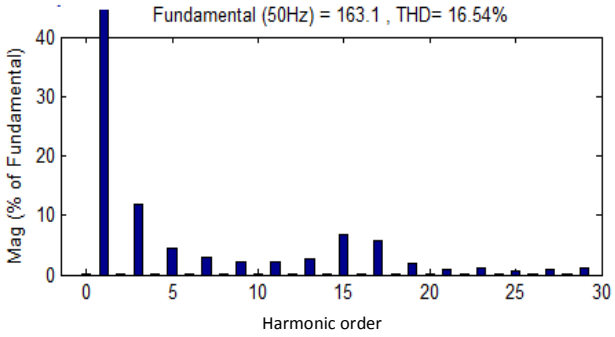

Fig.6.b. FFT analysis of the nine level inverter output voltage waveform (V_{AO}) based on ECSA

From the spectrum analysis, it is inferred that the THD Newton Raphson based is 8.28% and that for ECSA technique is 16.54%.

In figures 5b, when NR algorithm is applied, it is clearly identified that the 5^{th}, 7^{th} and the 11^{th} harmonics are completely eliminated, which explains the significant improvement in harmonic profile. However, Figure 6.a and figure 6.b represent the nine levels inverter output voltage and its FFT analysis respectively, obtained based on ECSA technique. Figure 6.b reveals harmonics 5, 7 and 11 in entirety, reason why the THD is higher than that obtained based on NR, hence an output voltage waveform represent a poor quality signal. In fact the higher harmonic range in ECSA technique is explained by the absence of the

optimization technique in order to eliminate, 5^{th}, 7^{th} and 11^{th} harmonics.

V. EXPREMENTAL RESULTS

The SPARTAN 6 VHDL program is verified and simulated using Xilinx-ISE 13.1 software [13]. Once the program is dumped on the FPGA kit, it acts as a controller and generates gating pulses given in figure 7.

The output of the gating signals can be observed in digital storage oscilloscope (DSO) as given in figure 8, where gating signals are generated based on NR algorithm.

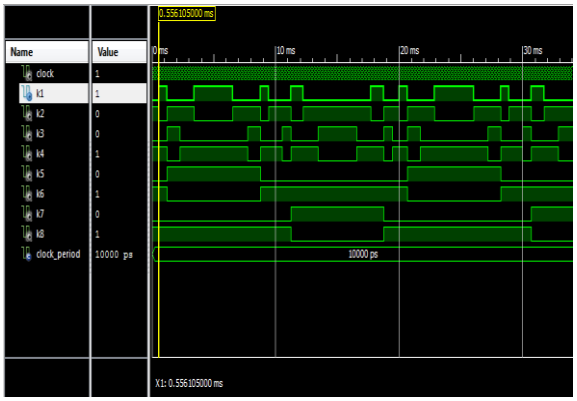

Fig.7 VHDL test bench simulation of the nine levels inverter power switches control signals (K1- K8)

Fig.8 Photograph of the DSO display the control signals based on NR and generated from FPAG- XILINX

VI. CONCLUSION

In this paper, the objectives are achieved by eliminating the 5^{th}, 7^{th} and 11^{th} harmonics of the output voltage. Simulation results prove the precision and efficiency of the NR algorithm compared to ECSA. Newton Raphson switching angles results are tested on a prototype model to validate selective harmonic elimination for cascaded asymmetrical nine levels inverter control. Comparison between gating signals of hardware implementation and simulation results discloses that hardware results closely agree with those of simulation.

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